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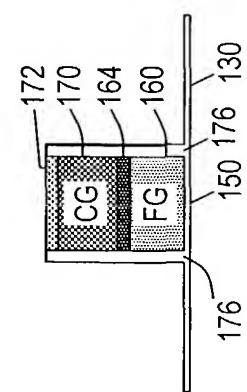


FIG. 1
PRIOR ART

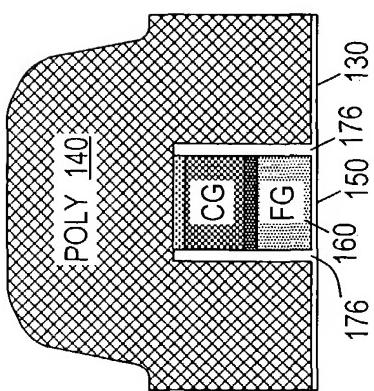


FIG. 2
PRIOR ART

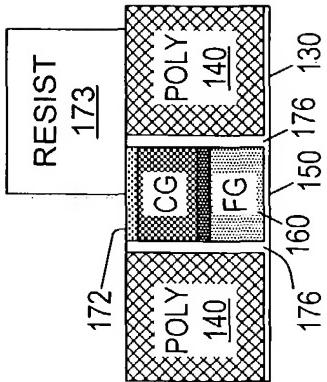


FIG. 3
PRIOR ART

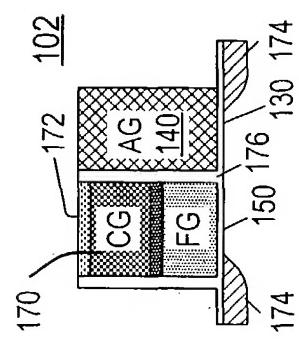


FIG. 4
PRIOR ART

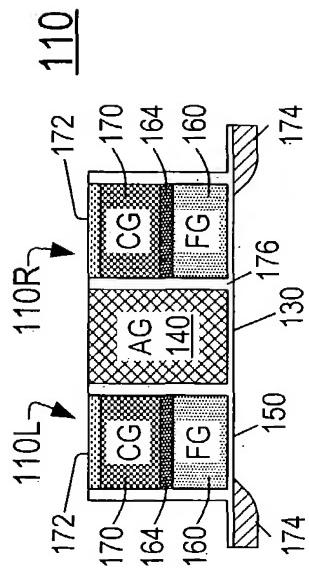


FIG. 5
PRIOR ART

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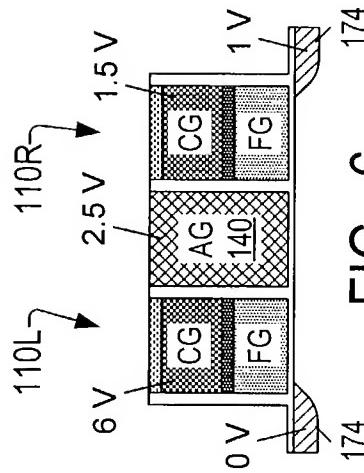
Read 110R

FIG. 6
PRIOR ART

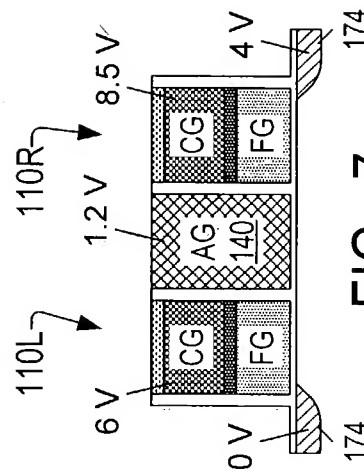
Program 110R

FIG. 7
PRIOR ART

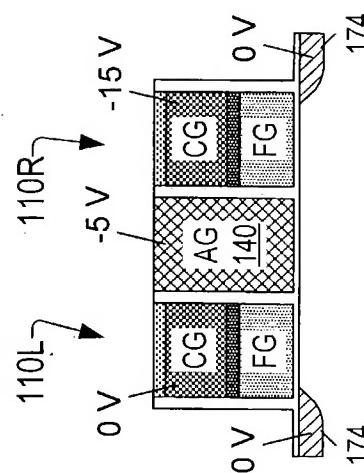
Erase 110R

FIG. 8
PRIOR ART

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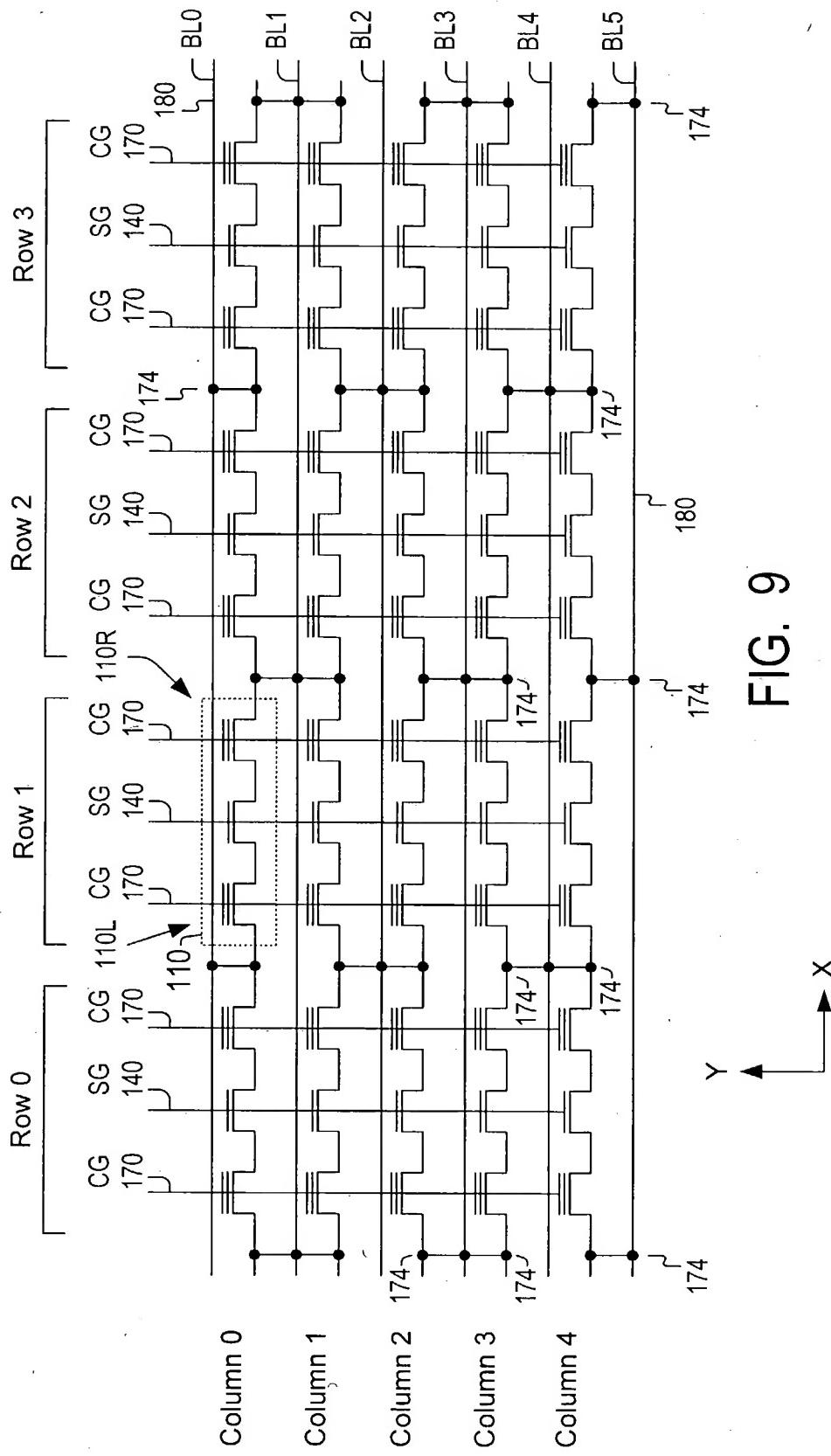
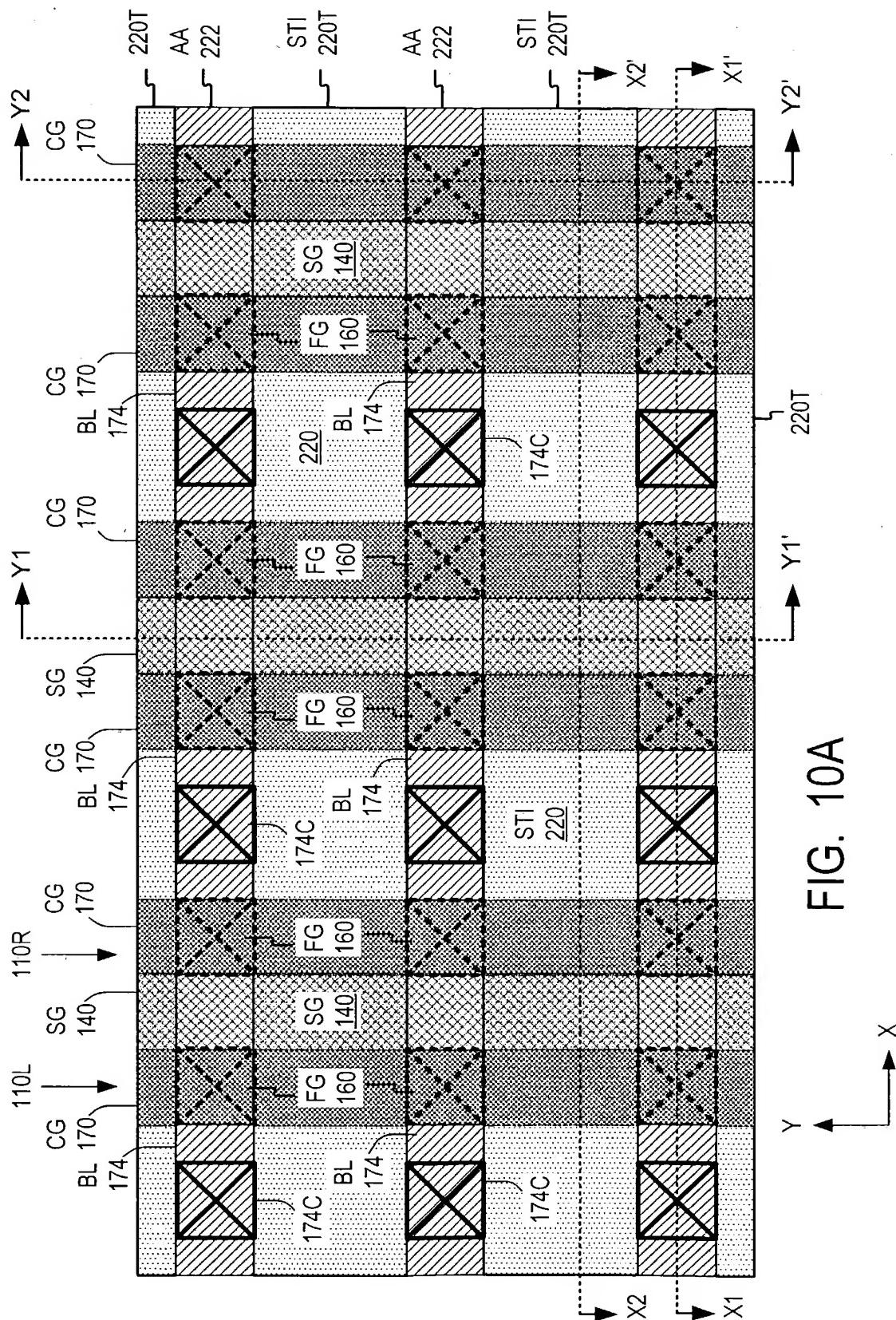


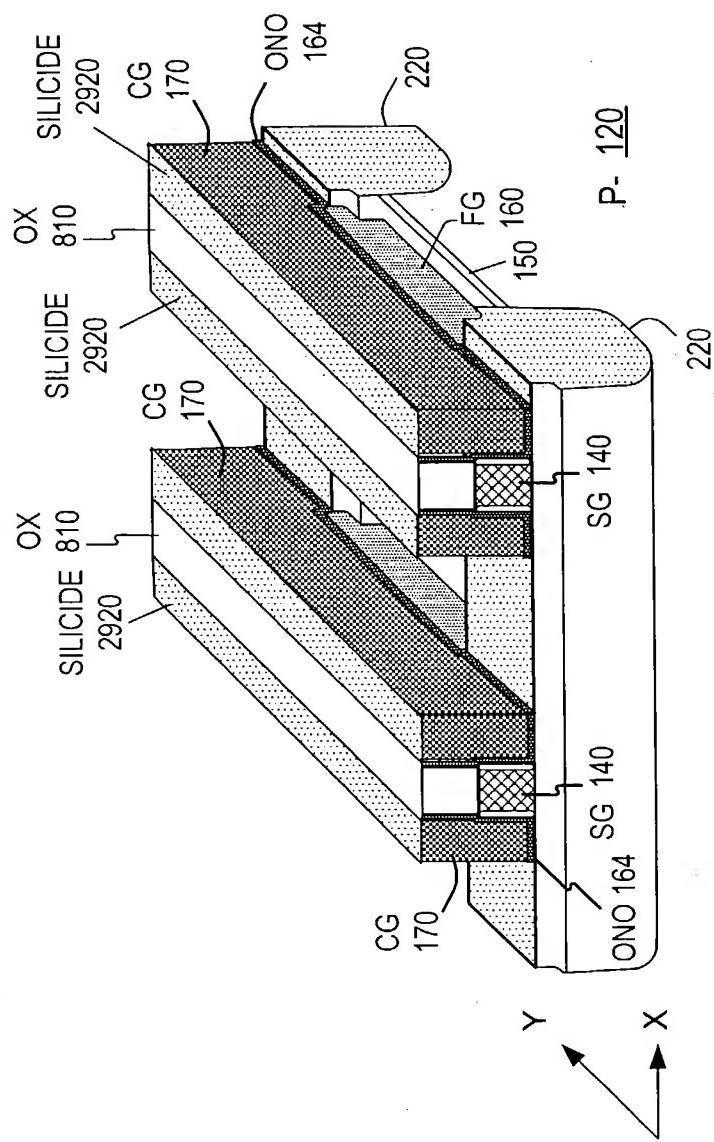
FIG. 9

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FIG. 10B



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FIG. 11 (Y1-Y1')

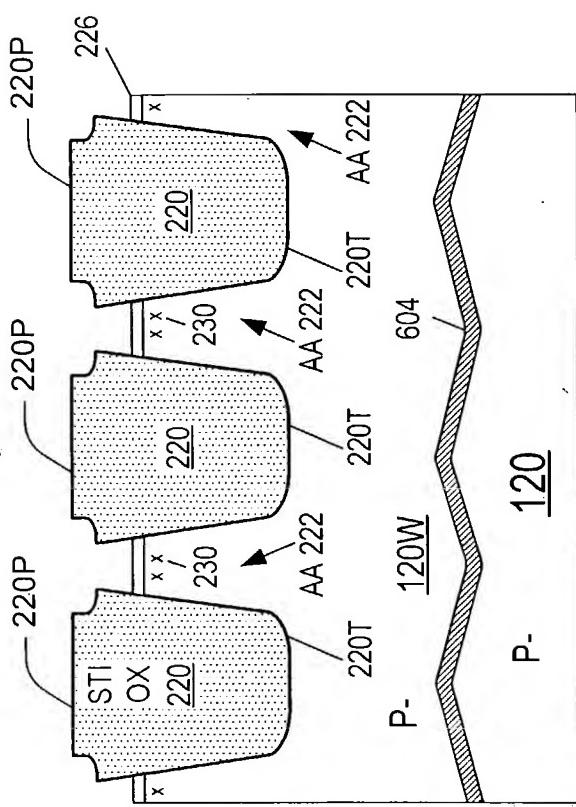
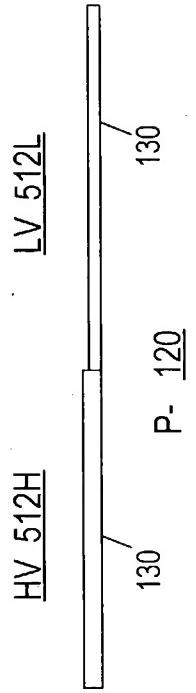
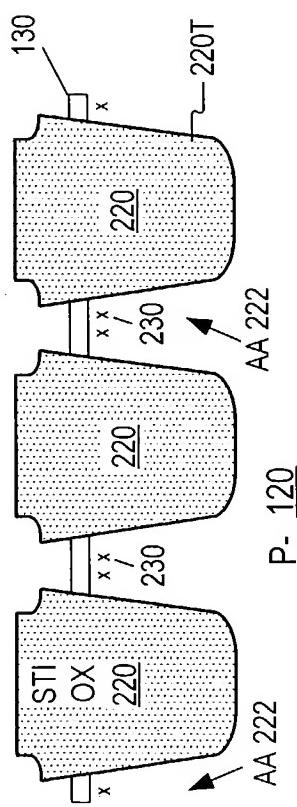
FIG. 12B
(PERIPHERY)

FIG. 12A (Y1-Y1')



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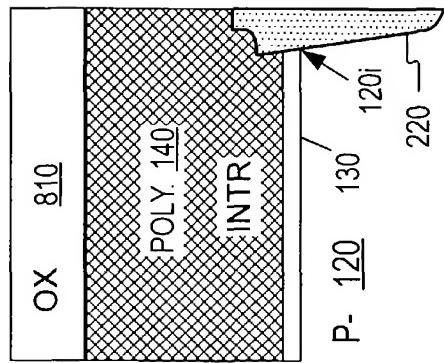


FIG. 13B
(PERIPHERY)

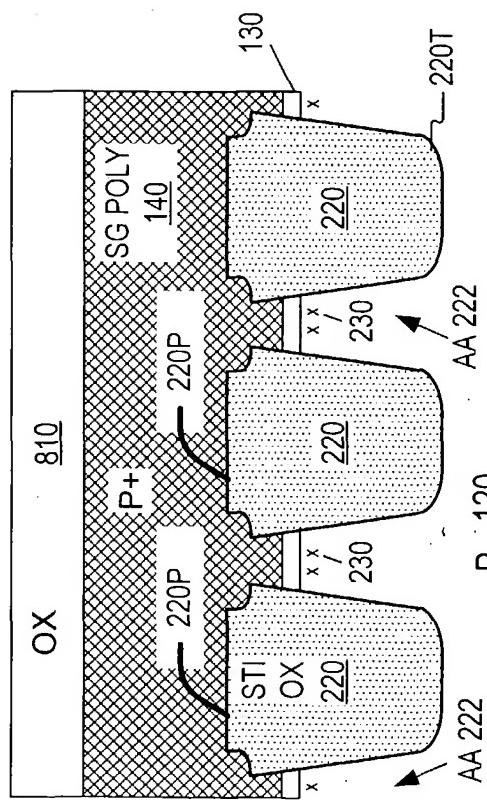
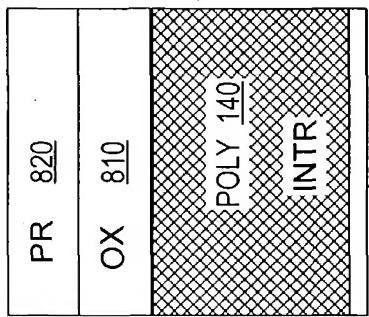


FIG. 13A (Y1-Y1')

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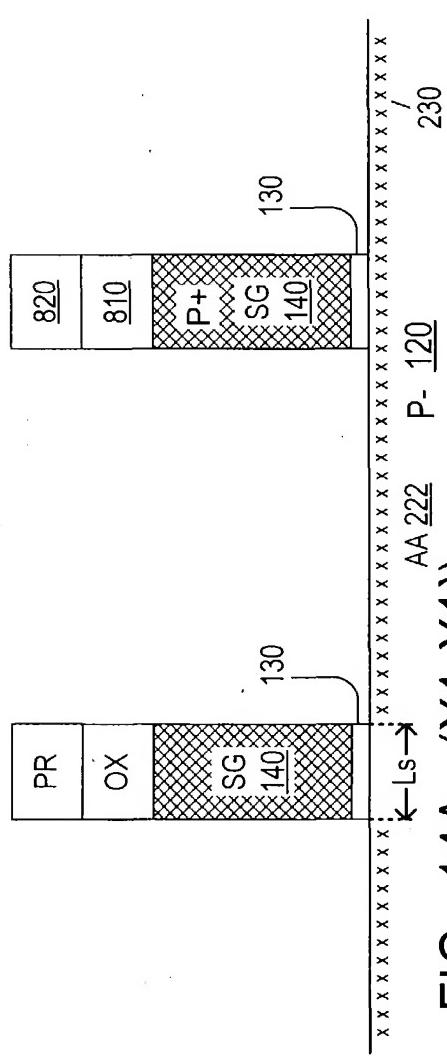
FIG. 14B
(PERIPHERY)

FIG. 14A (X1-X1')

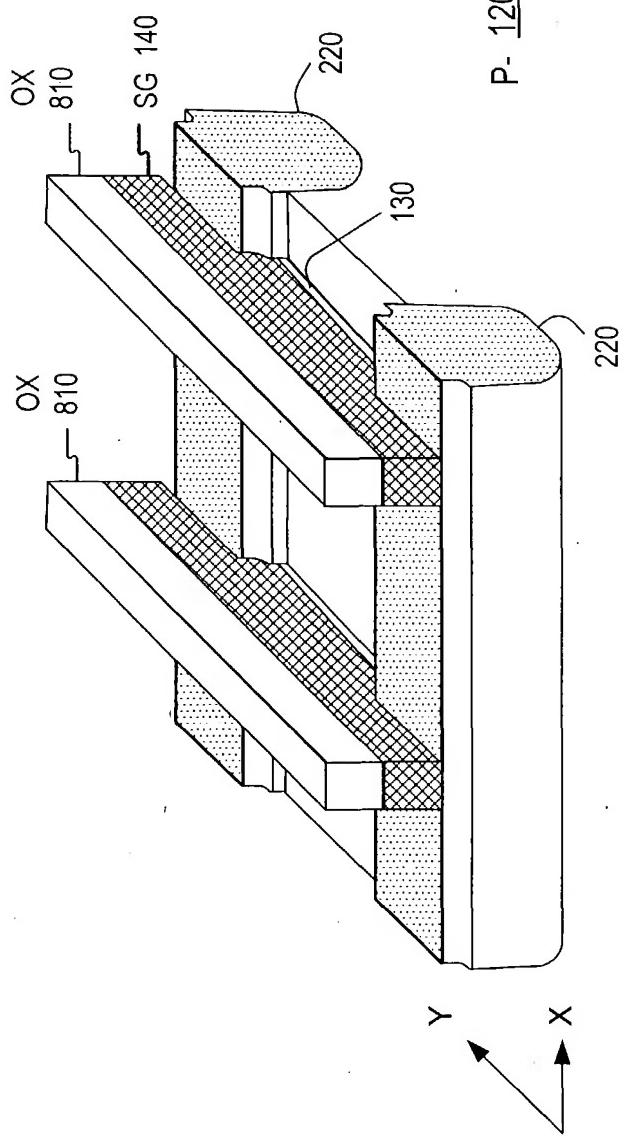
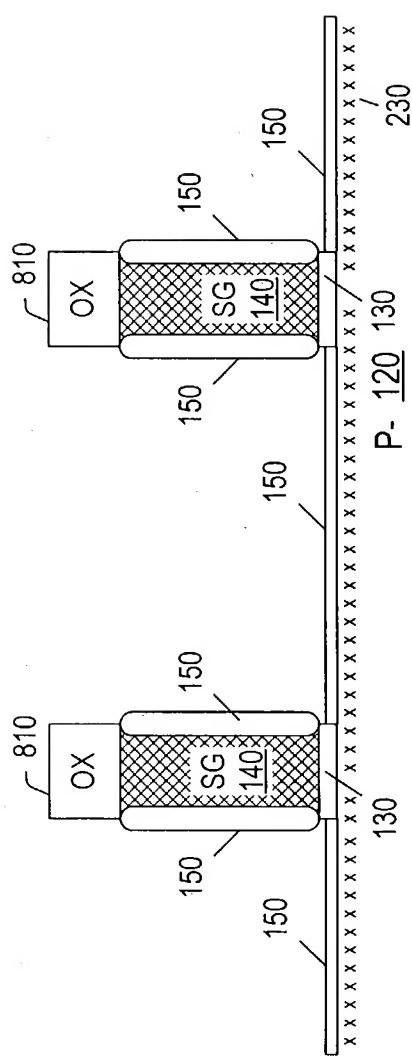
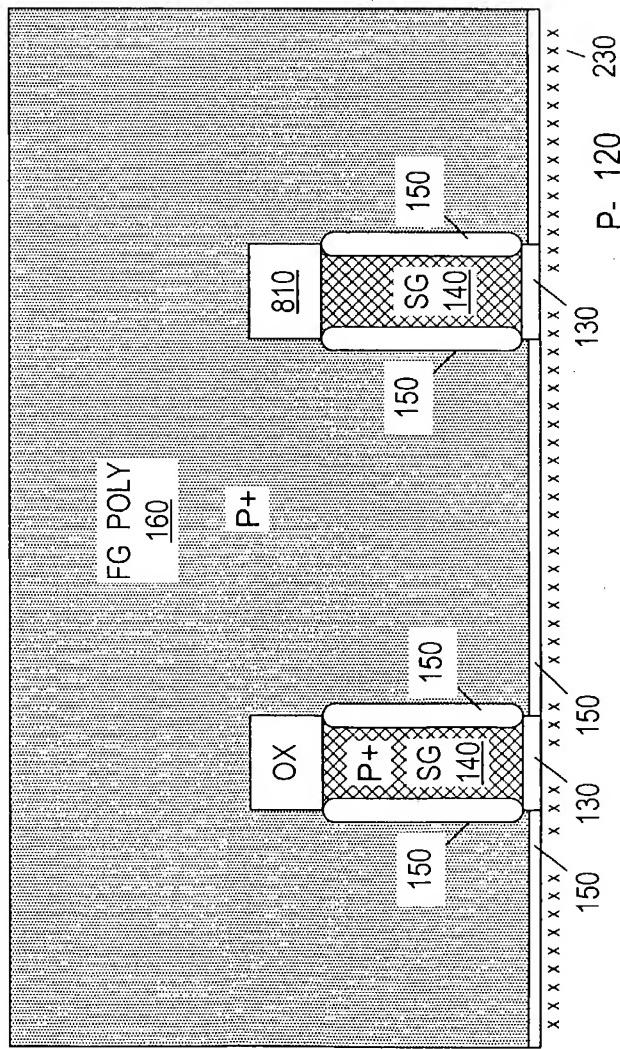


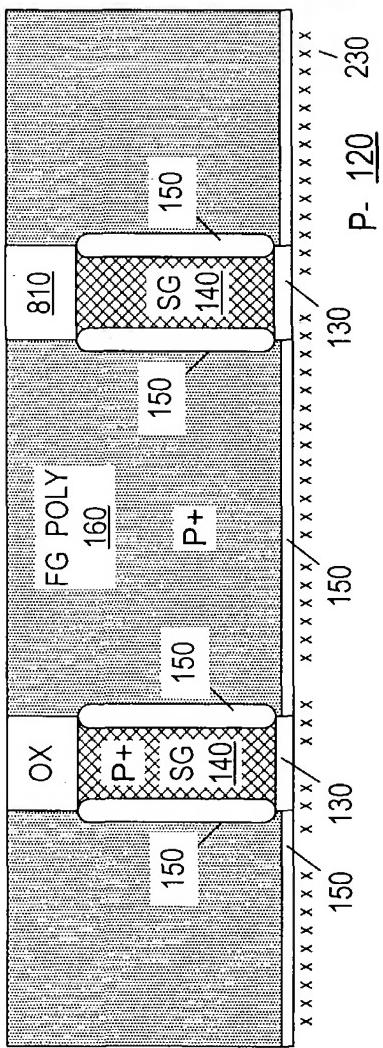
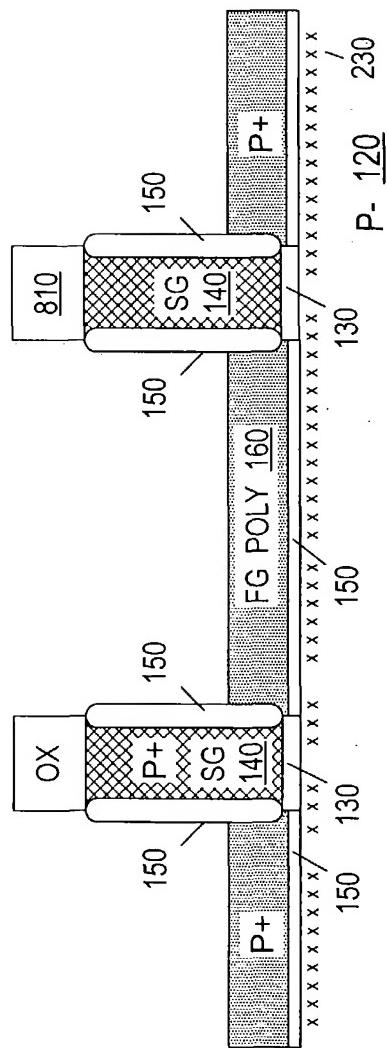
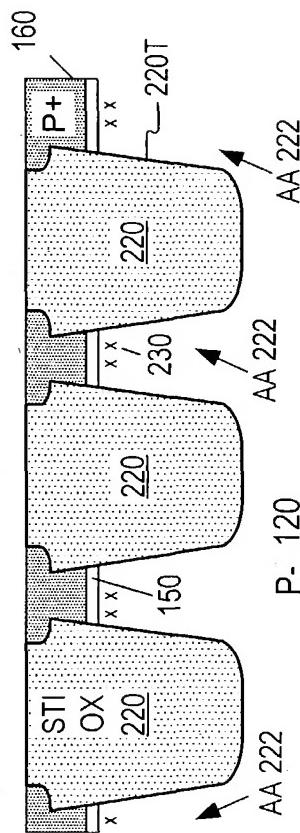
FIG. 15



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FIG. 16
(X1-X1')FIG. 17
(X1-X1')

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FIG. 18
(X1-X1')**FIG. 19A**
(X1-X1')**FIG. 19B**
(Y2-Y2')

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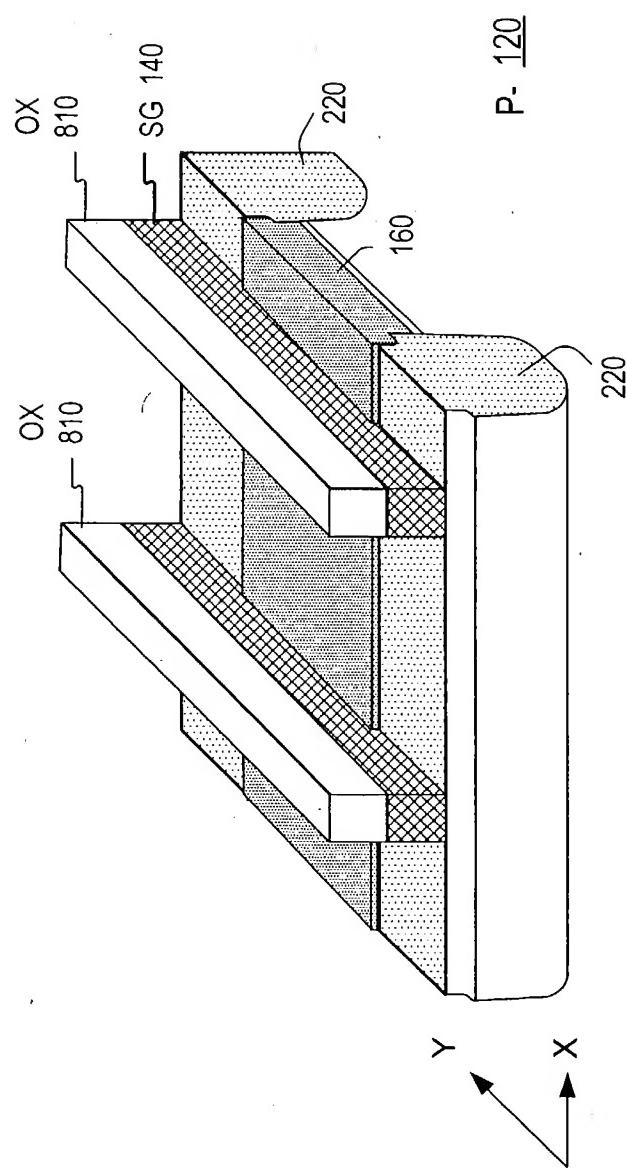
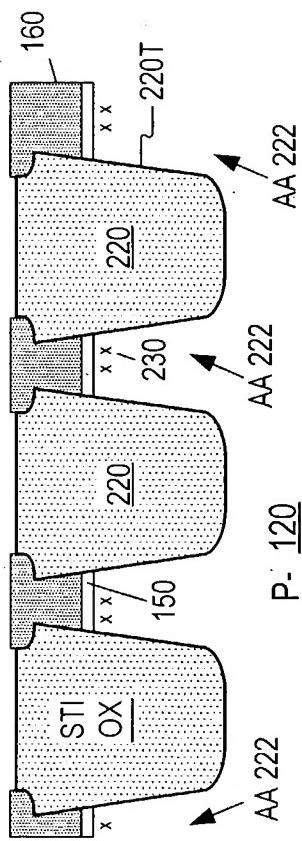
FIG. 20A
(Y2-Y2')

FIG. 20B

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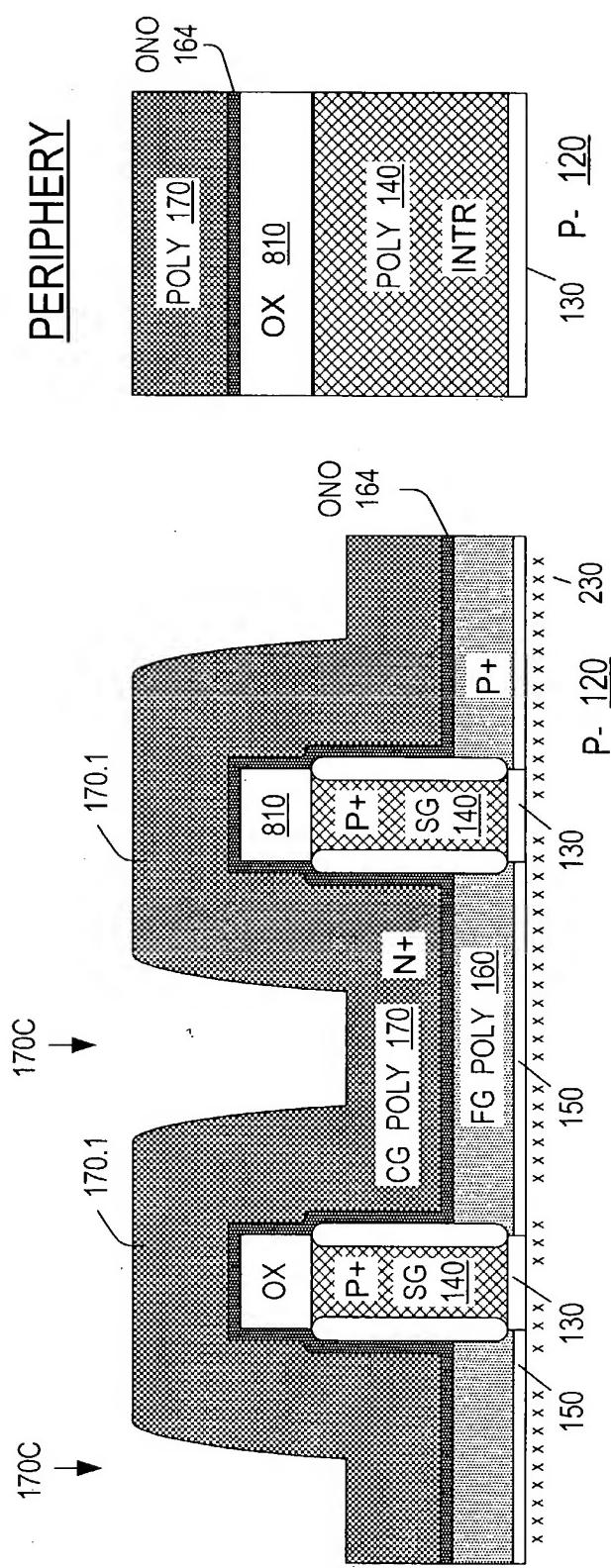


FIG. 21B

FIG. 21A (X1-X1')

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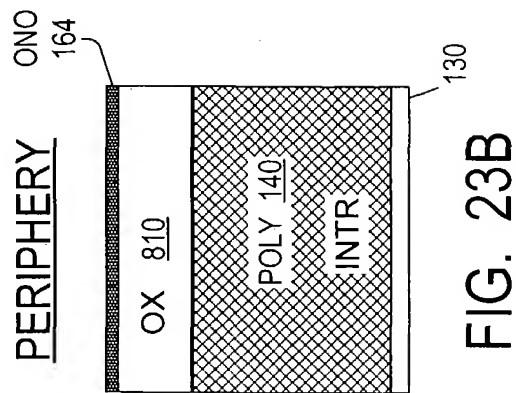
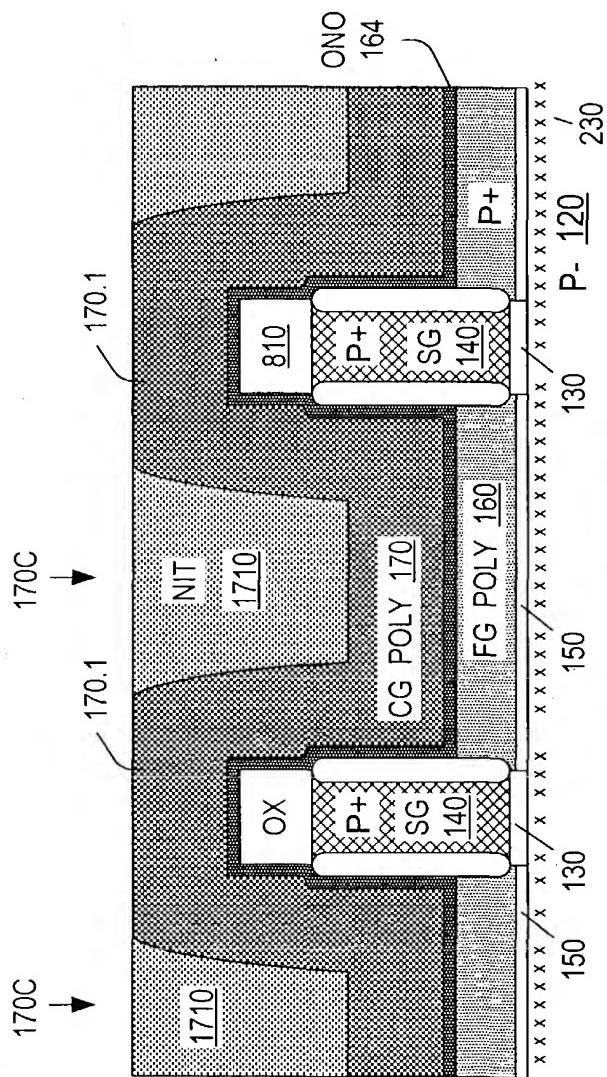
FIG. 22
(X1-X1')

FIG. 23B

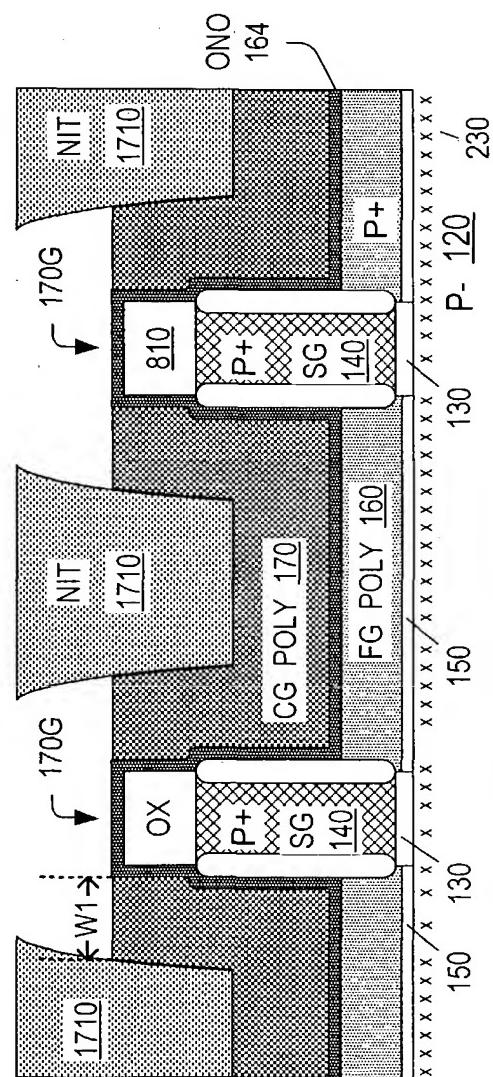
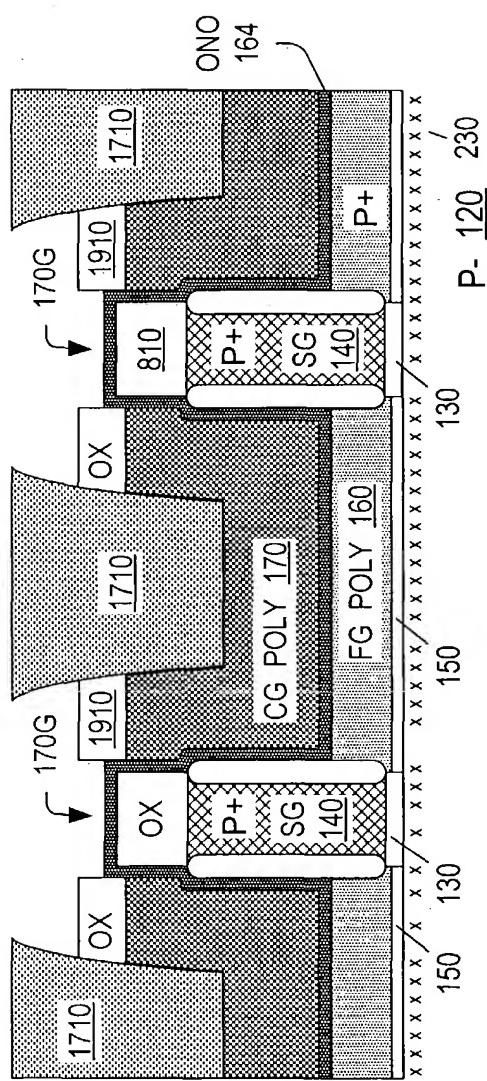
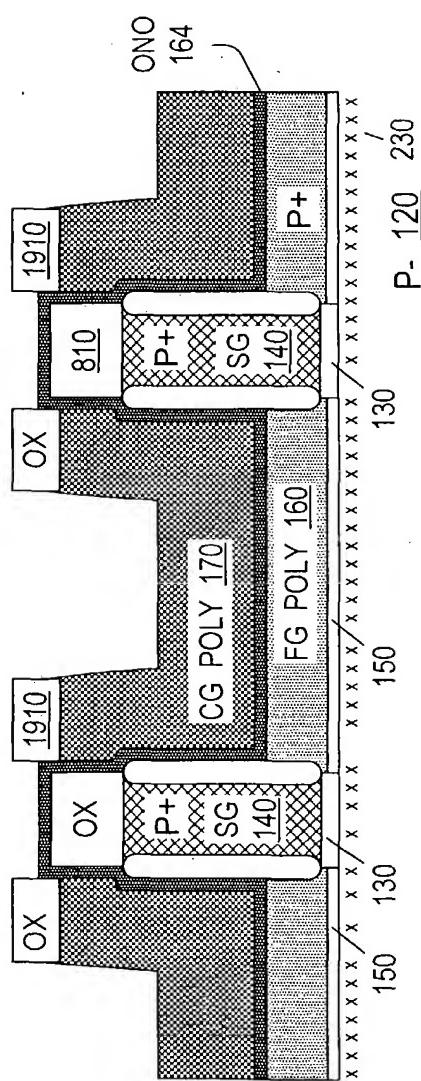
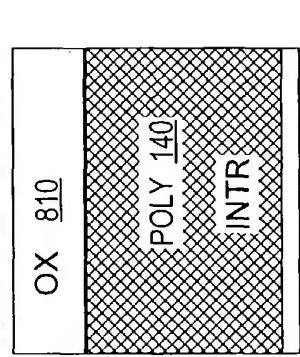
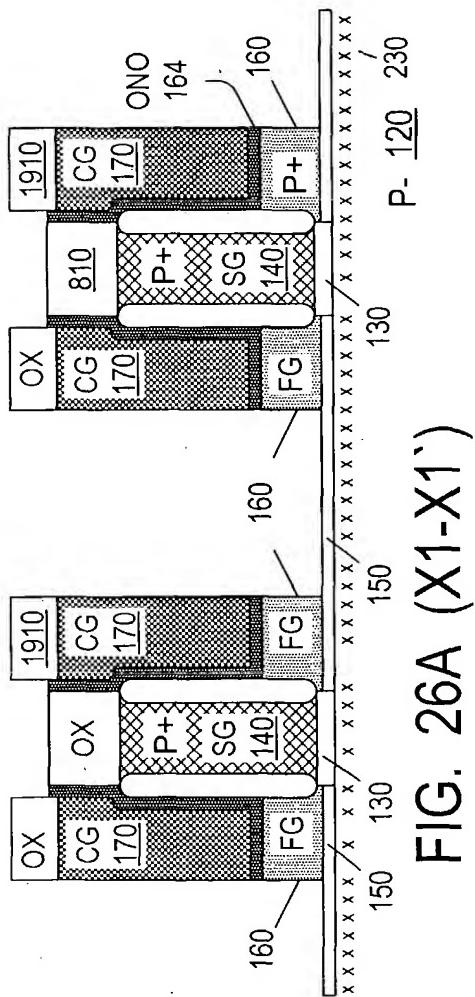
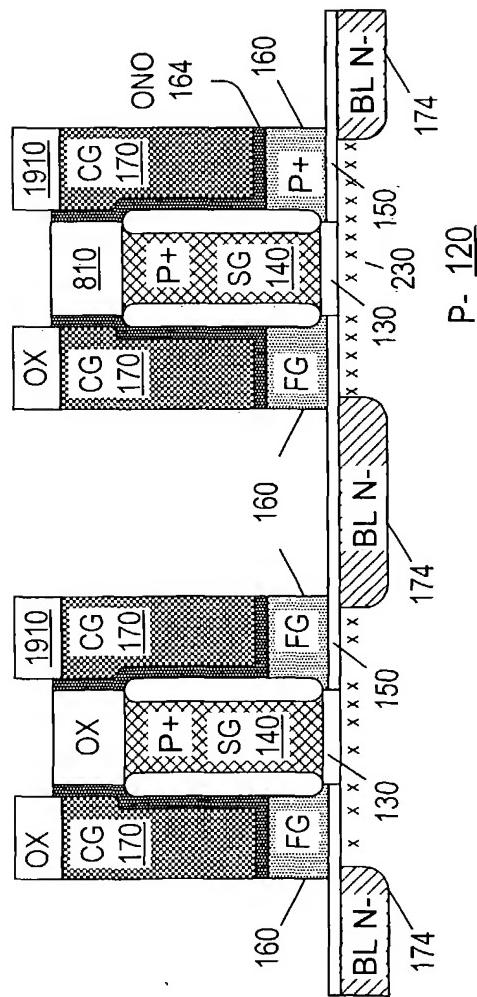


FIG. 23A (X1-X1')

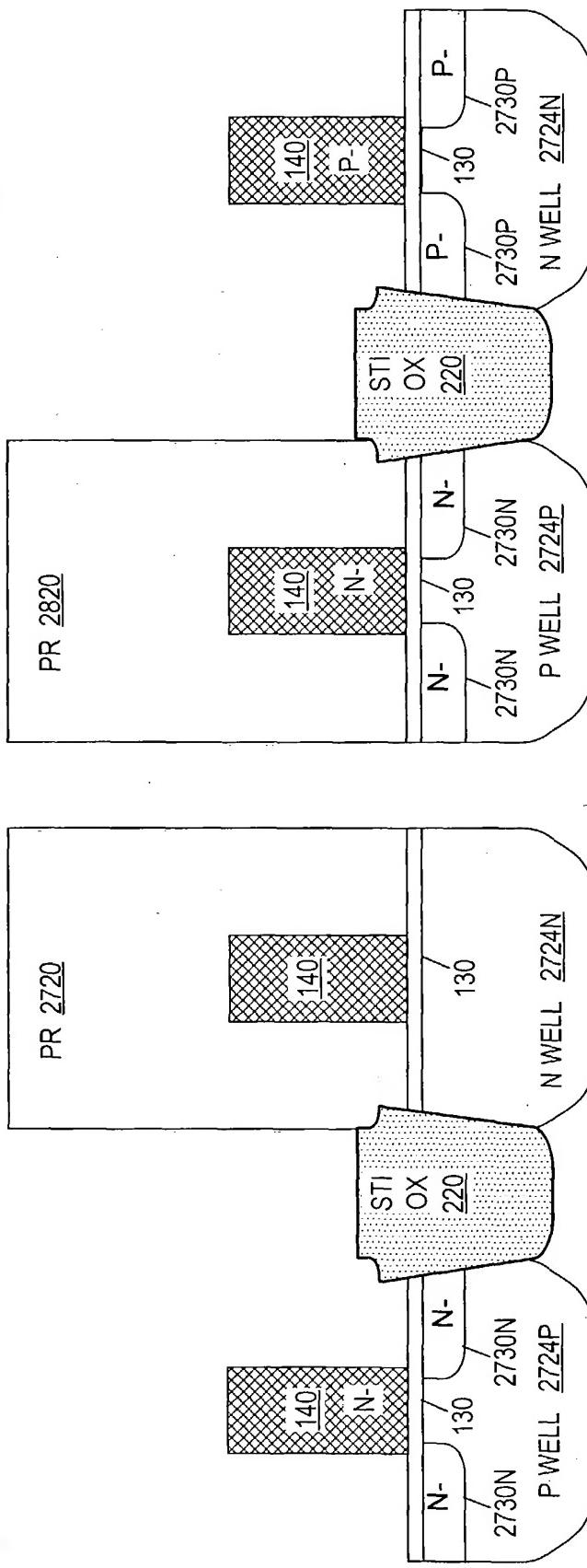
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FIG. 24
(X1-X1')FIG. 25
(X1-X1')

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PERIPHERY**FIG. 26B****FIG. 26A (X1-X1')****FIG. 27A
(X1-X1')**

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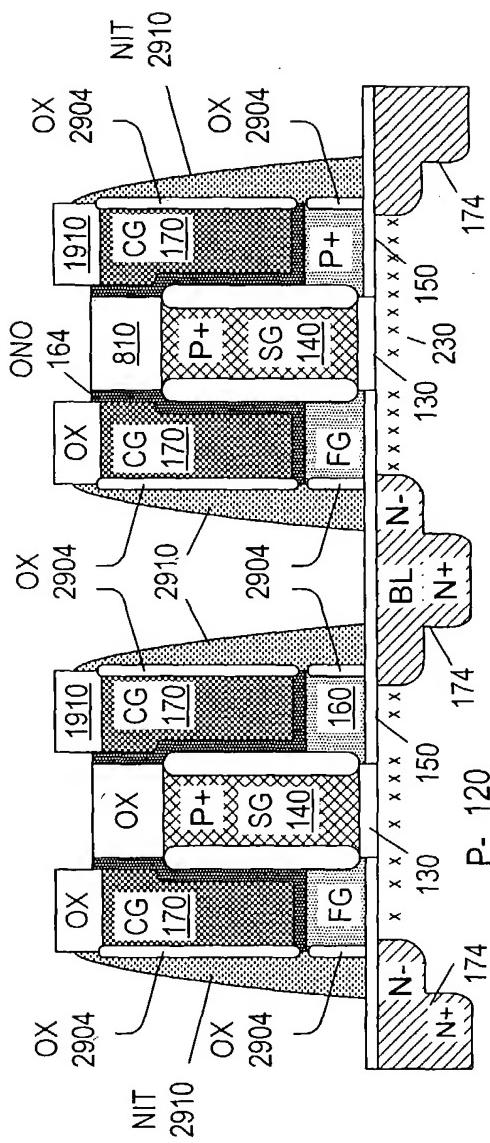
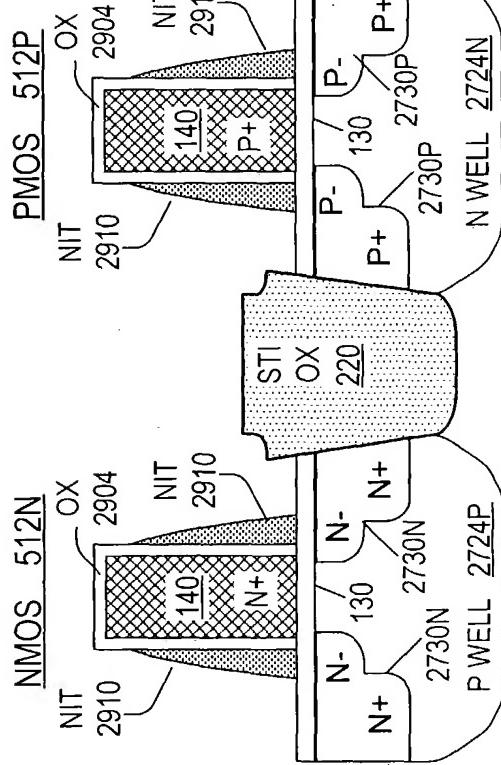
PMOS 512PNMOS 512NPMOS 512PNMOS 512N

P- 120

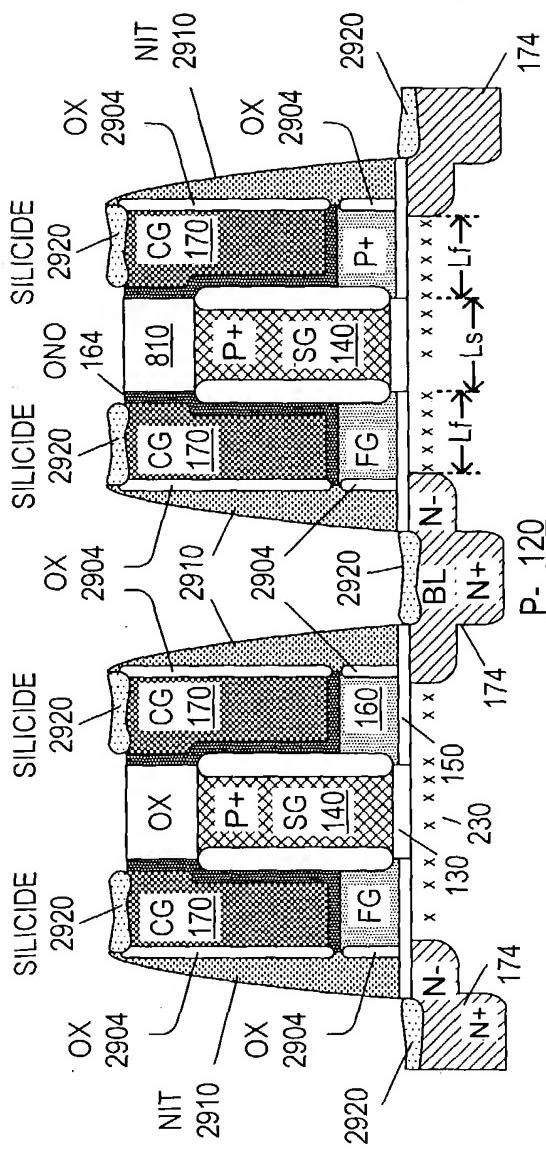
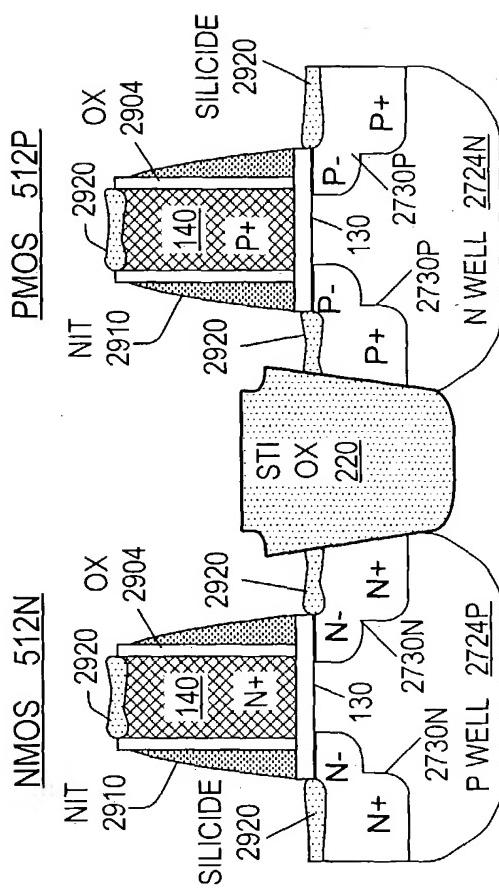
P- 120

FIG. 28
(PERIPHERY)FIG. 27B
(PERIPHERY)

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FIG. 29A
(X1-X1')FIG. 29B
(PERIPHERY)

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FIG. 30A
(X1-X1')**FIG. 30B**
(PERIPHERY)

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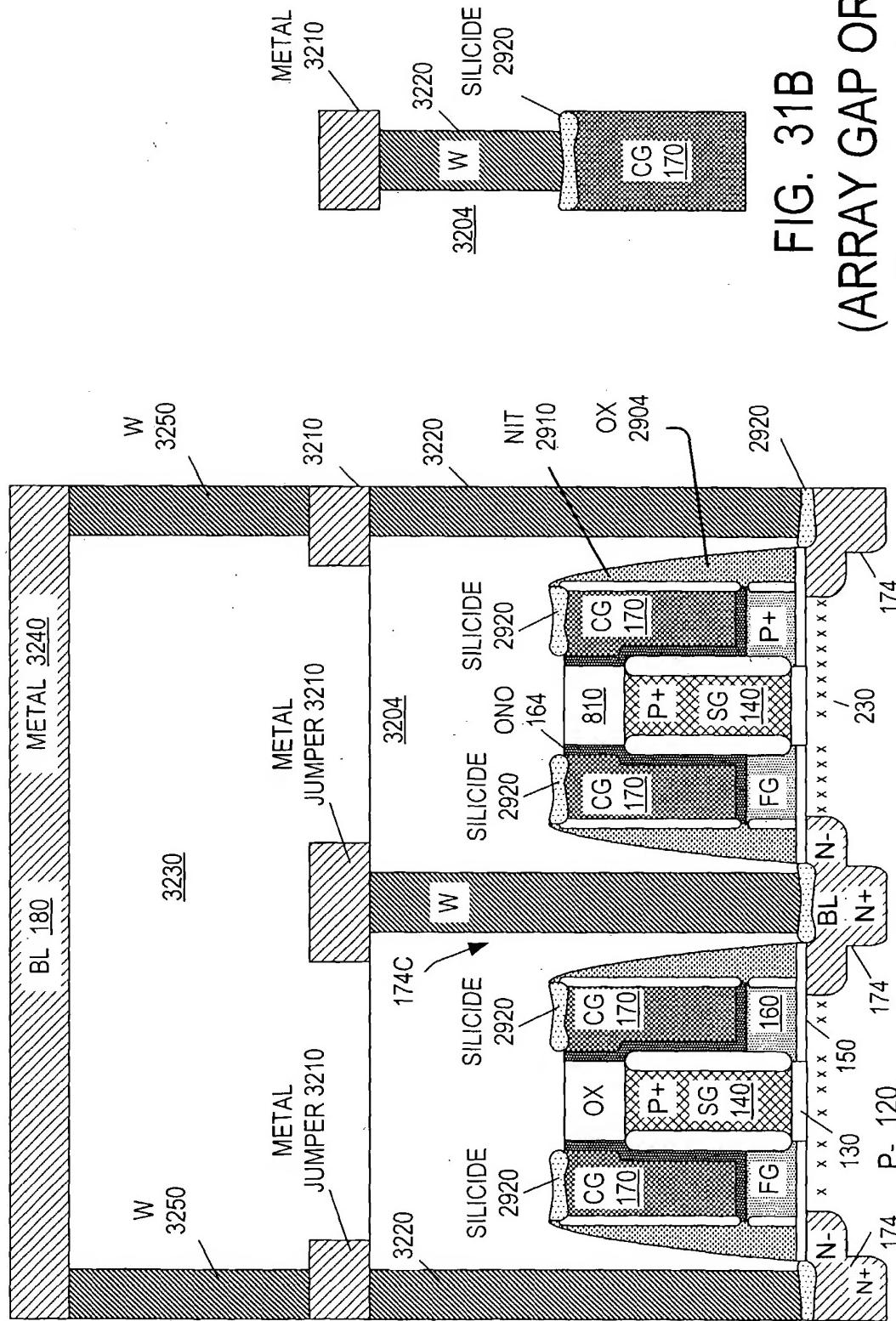


FIG. 31A (X_1-X_1')

FIG. 31B
(ARRAY GAP OR
BOUNDARY)

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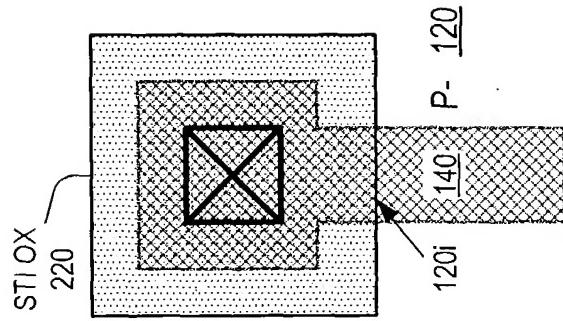


FIG. 31E
(PERIPHERY)

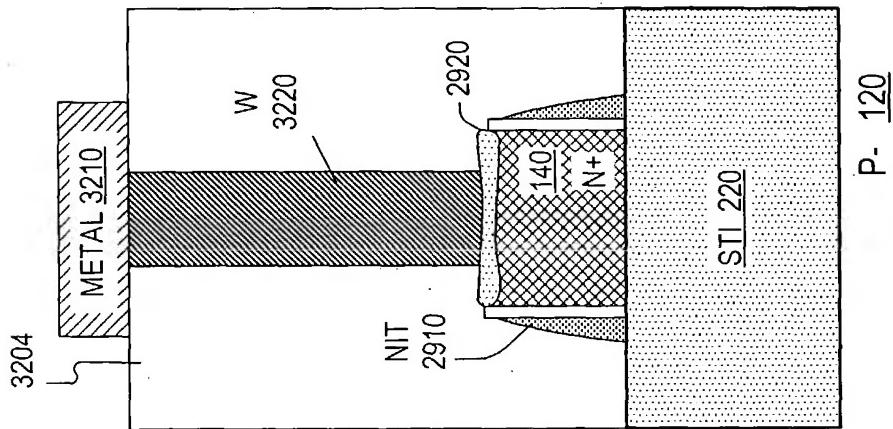


FIG. 31D
(PERIPHERY)

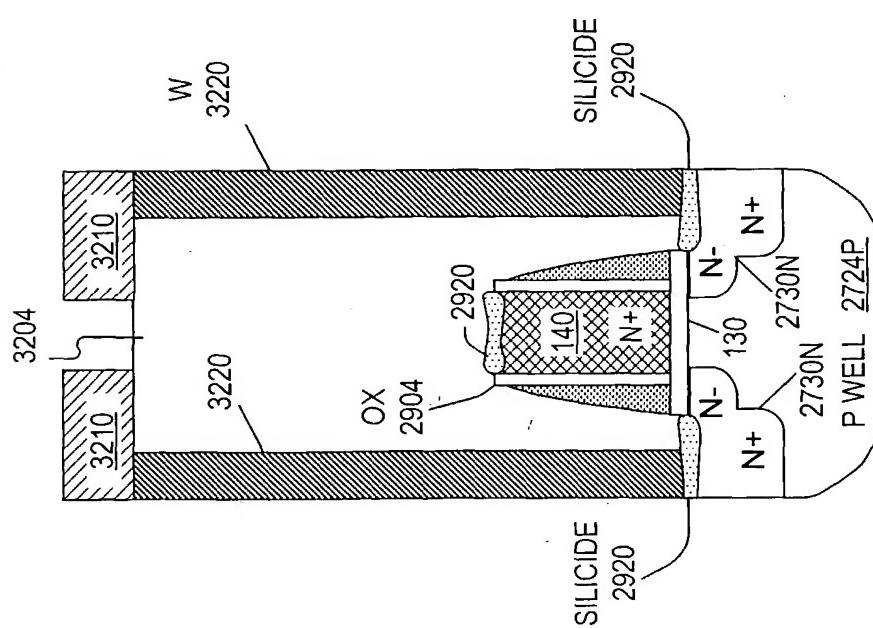


FIG. 31C
(PERIPHERY)

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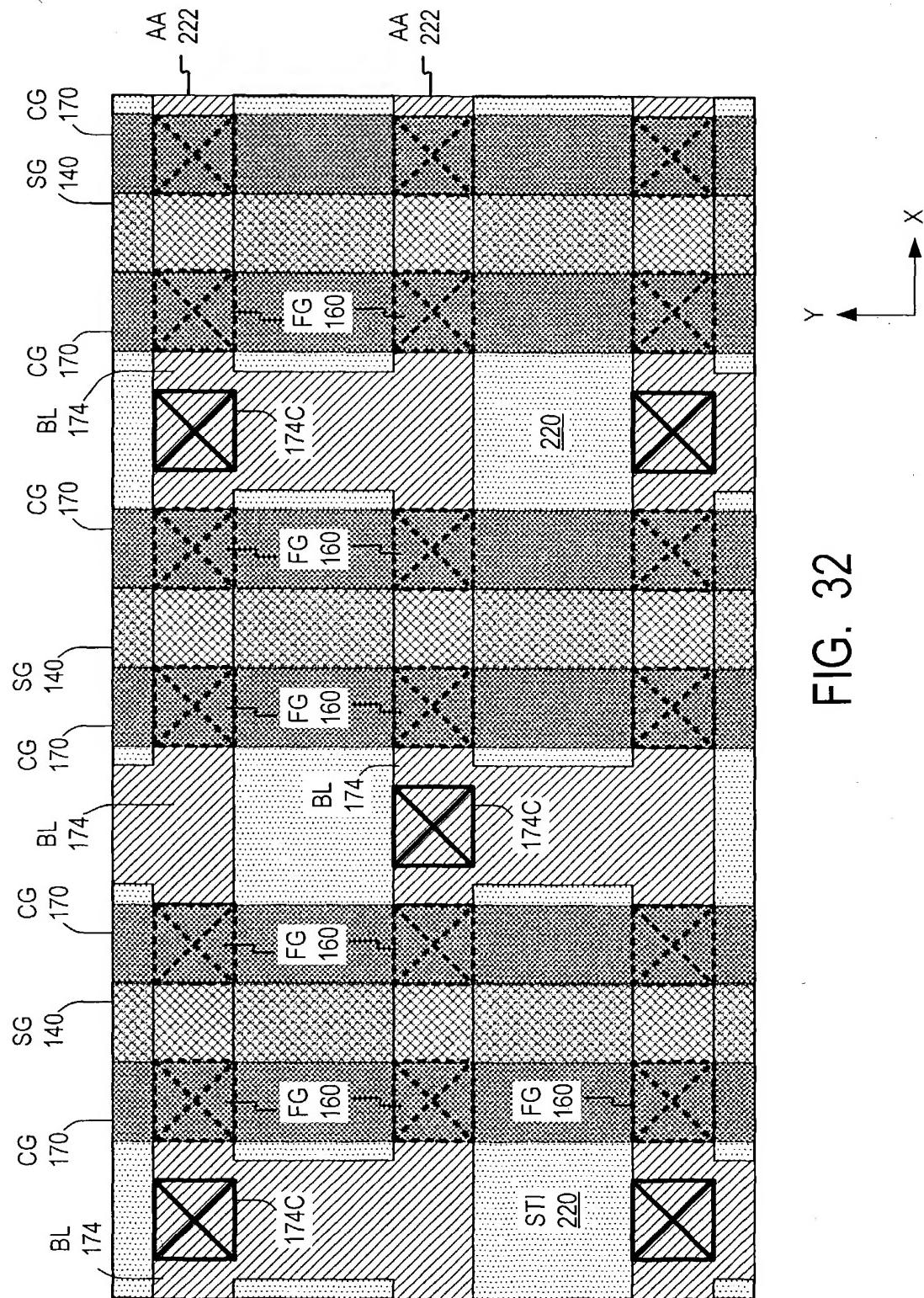


FIG. 32